Microprocessing and Microprogramming 39 (1993) 289–291
North-Holland

Author index to volume 39

Adams, R.G., *see* Steven, F.L. 75– 78
Alastruey, C.F. and J.R. González de Mendívil, Advances in adaptive simulation of interconnected systems with delays 201–204
Alvarez, A., *see* Guerra, F. 111–114
Antola, A., F. Distante and A. Marchese, High level synthesis through folding of data flow graphs: Optimal intra-node scheduling 89– 92
Arévalo, S., *see* Guerra, F. 111–114

Barrena, M., *see* Hernández, J. 65– 68
Benson, T.J.G., *see* Milligan, P. 129–132
Betts, A.K., I. Bolsens, E. Sicard, M. Renaudin and A. Johnstone, SMILE: A scalable microcontroller library element 259–263
Bisdounis, L., D.E. Metafas, A.M. Maras and C. Mavridis, VLSI implementation of digit-serial arithmetic modules 251–254
Blazek, Z., Monitoring and data recording system for the underground 281–284
Blom, F.C., J. Oliver, M. Rullán and C. Ferrer, Testability enhancement using physical design rules in a CMOS cell library 245–248
Bluemke, U., *see* Sosnowski, J. 115–118
Bolsens, I., *see* Betts, A.K. 259–263
Borzemski, L., D. Gajewski, S. Glowacz, M. Szczypinski and K. Wojtczak, A load balancing system for Unix-based local area networks 205–208
Britton, C., *see* Buchanan, M. 93– 96
Buchanan, M., B. Dickerson, C. Britton and M. Loomes, Using CCS for the specification of inheritance 93– 96

Calderón, J.C., J.R. Salvador, R. Valle, L. Paris and C. Ferrer, Multi-protocol communications controller 209–212
Carrabina, J., *see* Ribas, LI. 255–258
Cellary, W. and W. Wieczerzycki, Locking in DAG-structured databases 161–164
Cho, Y.H., *see* Kim, W.Y. 101–104
Cho, Y.H., *see* Lee, J.H. 105–108
Choi, K., *see* Shin, D. 173–176

de Miguel, P., *see* Hernández, J. 65– 68
del Campo, I., J.R. González de Mendívil and J.M. Tarela, Development of a fuzzy logic controller on a digital signal processor 277–280
del Rio, A. and P. Mariño, A rule based programming language for real-time applications 139–142
del Rio, A., *see* Mariño, P. 187–190

Dékány, A., I. Erényi and S. Fejes, High speed parallel implementation of the statistical feature matrix method 285–288
Derezińska, A., *see* Sosnowski, J. 115–118
Dibuz, S., A frame-based approach to conformance testing 191–194
Dickerson, B., *see* Buchanan, M. 93– 96
Distante, F., *see* Antola, A. 89– 92

Economou, G.-P., S.S. Nikolaidis, D.E. Metafas and C.E. Goutis, Development of a technology independent library 241–244
Erényi, I., *see* Dékány, A. 285–288

Fejes, S., *see* Dékány, A. 285–288
Fernandez, B., *see* Wu, J. 43– 53
Ferrer, C., *see* Blom, F.C. 245–248
Ferrer, C., *see* Calderón, J.C. 209–212
Frey, M. and A. Weininger, Using temporal logic specifications to debug parallel programs 97–100

Gaál, T., Parallel compiler generation 147–150
Gajewski, D., *see* Borzemski, L. 205–208
Gámez, J.A., *see* Moreno, G. 169–172
Glowacz, S., *see* Borezemski, L. 205–208
Gómez, L., A. Hernández and A. Nunez, Multiobjective optimization using analytical models of GaAs high-speed digital circuits 267–270
González de Mendívil, J.R., *see* Alastruey, C.F. 201–204
González de Mendívil, J.R., *see* del Campo, I. 277–280
González, A., *see* Tubella, J. 83– 86
González, P., *see* Moreno, G. 169–172
Goutis, C.E., *see* Economou, G.-P. 241–244
Guerra, F., S. Arévalo, A. Alvarez and J. Miranda, A quick distributed consensus protocol 111–114

Hausen, H.-L., *see* Welzel, D. 273–277
He, H. and H. Zedan, Cycle calculus for hybrid systems 223–228
Hermida, R., *see* Moreno, R. 233–236
Hernández, A., *see* Gómez, L. 267–270
Hernández, J., P. de Miguel, M. Barrena, J.M. Martínez, A. Polo and M. Nieto, Implementation details of ALBA in a transputer machine 65– 68
Hohl, W., *see* Pataricza, A. 69– 74
Hönig, J., *see* Pataricza, A. 69– 74
Horvat, T., *see* Kapus, T. 143–146

Jávor, A. and Á. Vigh, Conflict handling in high level Petri nets 133–136
Jeong, D.-K., *see* Kim. S.B. 1– 15
Jerman-Blažič, B., *see* Trček, D. 183–186
Johnstone, A., *see* Betts, A.K. 259–263
Jorba, A., *see* Larriba-Pey, J.-L. 125–128

Kacsuk, P., Memory management in LOGFLOW 79– 82
Kalinowski, T., *see* Thor, M. 59– 64
Kameas, A., *see* Papadimitriou, S. 119–124
Kandus, G., *see* Pučko, M. 195–198
Kapus, T., B. Horvat and M. Pučko, A true concurrency semantics for parallel programs 143–146
Kapus-Kolar, M., Derivation of protocols implementing services with event priorities 213–216
Kim, B. and S. Moon, A flexible indexing structure supporting multi-attribute database applications: MAIN 177–180
Kim, C.S., *see* Kim, S.B. 1– 15
Kim, M.H., *see* Lee, D.H. 165–168
Kim, M.H., *see* Lee, J.H. 105–108
Kim, S.B., M.S. Park, S.-H. Park, S.L. Min, H. Shin, C.S. Kim and D.-K. Jeong, Threaded prefetching: An adaptive instruction prefetch mechanism 1– 15
Kim, W.Y., Y.J. Lee, J.H. Lee and Y.H. Cho, The fuzzy set model based on *n*-ary positively compensatory operators 101–104

Larriba-Pey, J.-L., A. Jorba and J.J. Navarro, Spike algorithm with savings for strictly diagonal dominant tridiagonal systems 125–128
Lee, D.H. and M.H. Kim, Extending semantics of relational operators for vague queries 165–168
Lee, J. and S. Moon, Architecture for interoperability of network management systems in multi-domain network 217–220
Lee, J.H., *see* Kim, W.Y. 101–104
Lee, J.H., M.H. Kim and Y.H. Cho, Using term dependencies of a thesaurus in the fuzzy set model 105–108
Lee, Y.J., *see* Kim, W.Y. 101–104
Loomes, M., *see* Buchanan, M. 93– 96

Majzik, I., *see* Pataricza, A. 69– 74
Maras, A.M., *see* Bisdounis, L. 251–254
Marchese, A., *see* Antola, A 89– 92
Marino, P. and A. del Rio, An accurate and fast CSMA/CD simulator 187–190
Mariño, P., *see* del Rio, A. 139–142
Martinez, J.M., *see* Hernández, J. 65– 68
Mavridis, C., *see* Bisdounis, L. 251–254
McConnell, R., *see* Milligan, P. 129–132
Metafas, D.E., *see* Bisdounis, L. 251–254
Metafas, D.E., *see* Economou, G.-P. 241–244
Milligan, P., T.J.G. Benson, R. McConnell and A. Rea, Process to processor mapping within the Mathematician's Devil 129–132
Min, S.L., *see* Kim, S.B. 1– 15
Miranda, J., *see* Guerra, F. 111–114
Moon, S., *see* Kim, B. 177–180
Moon, S., *see* Lee, J. 217–220
Moon, S., *see* Nam, H. 155–158
Moreno, G., P. González and J.A. Gámez, Parallel algorithm for table division in relational databases 169–172
Moreno, R., *see* Olcoz, K. 263–266
Moreno, R., R. Hermida, D. Mozos and K. Olcoz, Global hardware synthesis guided by realistic probability computation 233–236
Mozos, D., *see* Moreno, R. 233–236
Mozos, D., *see* Olcoz, K. 263–266

Nam, H. and S. Moon, Global deadlock detection for concurrency control in multidatabase systems 155–158
Navarro, J.J., *see* Larriba-Pey, J.-L. 125–128
Nieto, M., *see* Hernández, J. 65– 68
Nikolaidis, S.S., *see* Economou, G.-P. 241–244
Nunez, A., *see* Gómez, L. 267–270

Olcoz, K., *see* Moreno, R. 233–236
Olcoz, K., F. Tirado, D. Mozos, J. Septien and R. Moreno, Data path structures and heuristics for testable allocation in high level synthesis 263–266
Oliver, J., *see* Blom, F.C. 245–248

Papadimitriou, S., A. Kameas and G. Pavlides, Determining effective multiprocessor scheduling policies for repetitive real-time tasks 119–124
París, L., *see* Calderón, J.C. 209–212
Park, M.S., *see* Kim, S.B. 1– 15
Park, S.-H., *see* Kim, S.B. 1– 15
Pataricza, A., I. Majzik, W. Hohl and J. Hönig, Watchdog processors in parallel systems 69– 74
Pavlides, G., *see* Papadimitriou, S. 119–124
Pérez, J.M., *see* Ribas, Ll. 255–258
Petrou, L.P., *see* Spais, V.A. 17– 23
Polo, A., *see* Hernández, J. 65– 68
Pučko, M. and G. Kandus, Service-driven protocol synthesis for specific users 195–198
Pučko, M., *see* Kapus, T. 143–146

Rea, A., *see* Milligan, P. 129–132
Renaudin, M., *see* Betts, A.K. 259–263
Ria, A. and P. Marino, A rule based programming language for real-time applications 139–142
Ribas, Ll., J. Riera, J.M. Pérez, J. Saiz, J. Carrabina and Ll. Terés, Automatic pattern generation for the electrical characterization of digital modules 255–258
Riera, J., *see* Ribas, Ll. 255–258
Rullán, M., *see* Blom, F.C. 245–248

Saiz, J., *see* Ribas, Ll. 255–258
Salvador, J.R., *see* Calderón, J.C. 209–212
Sami, M.G., D. Sciuto and R. Stefanelli, Concurrently self-checking structures for FSMs 237–240
Sciuto, D., *see* Sami, M.G. 237–240
Septien, J., *see* Olcoz, K. 263–266
Shin, D., Y. Yoon and K. Choi, The performance evaluation of a knowledge-based information retrieval system 173–176

Shin, H., *see* Kim, S.B. 1– 15
Sicard, E., *see* Betts, A.K. 259–263
Sosnowski, J., A. Derezińska and I. Bluemke, Autodiagnostics for transputer systems 115–118
Spais, V.A. and L.P. Petrou, Implementation of the robot inverse dynamics computation algorithm on a transputer network 17– 23
Stefanelli, R., *see* Sami, M.G. 237–240
Steven, F.L., R.G. Adams, G.B. Steven, L. Wang and D.J. Whale, Addressing mechanisms for VLIW and superscalar processors 75– 78
Steven, G.B., *see* Steven, F.L. 75– 78
Su, B., J. Wang, Z. Tang, C. Zhang and W. Zhao, URPR-1: A single-chip VLIW architecture 25– 41
Švéda, M., Language prototyping with attribute grammars and macros 151–154
Szczypinski, M., *see* Borezemski, L. 205–208

Takken, R., *see* Withagen, W.J. 229–232
Tang, Z., *see* Su, B. 25– 41
Tarela, J.M., *see* del Campo, I. 277–280
Terés, Ll., *see* Ribas, Ll. 255–258
Thor, M. and T. Kalinowski, HP-MODTRANS: A high performance modular transputer architecture 59– 64
Tirado, F., *see* Olcoz, K. 263–266
Trček, D. and B. Jerman-Blažič, Certificates handling and their support within X.500 system 183–186
Tubella, J. and A. González, MEM: A new execution model for Prolog 83– 86

Valle, R., *see* Calderón, J.C. 209–212
Vigh, Á., *see* Jávor, A. 133–136

Wang, J., *see* Su, B. 25– 41
Wang, L., *see* Steven, F.L. 75– 78
Weininger, A., *see* Frey, M. 97–100
Welzel, D. and H.-L. Hausen, A five step method for metric-based software evaluation-effective software metrication with respect to quality standards 273–277
Whale, D.J., *see* Steven, F.L. 75– 78
Wieczerzycki, W., *see* Cellary, W. 161–164
Withagen, W.J. and R. Takken, Hierachical modeling and simulation of processor architectures 229–232
Wojtczak, A., *see* Borzemski, L. 205–208
Wu, J. and E.B. Fernandez, Broadcasting in faulty hypercubes 43– 53

Yoon, Y., *see* Shin, D. 173–176

Zedan, H., *see* He, H. 223–228
Zhang, C., *see* Su, B. 25– 41
Zhao, W., *see* Su, B. 25– 41

Microprocessing and Microprogramming 39 (1993) 293–294
North-Holland

Subject index to volume 39

ASIC 259
Actor-based languages 65
Adaptive simulations 201
Addressing mechanisms 75
Add/subtract cell 251
Allocation 233
Architecture 25
Attribute grammar 151
Automatic characterization 255
Automatic service implementation 213
Autoparallelization 129

Berger code 237
Binomial trees 43
Broadcasting 43

CCS 93
Concurrency control 155, 161
Conflicts 133
Conformance testing 191

Data path allocation 263
Data recording 281
Database systems 155, 177
Deadlock detection 155
Description language 229
Design for testability 263
Design space 233
Diagnosis 187
Diagnostics 281
Digit-serial arithmetic 251
Digital signal processing 277
Distributed systems 111, 195, 213
Distributed transparency 217
Division algorithms 251

Evaluation of software 273
Execution model 83
Expert systems 139, 187

Fault tolerant computing 69
Fault tolerant multiprocessing 43
Feature extraction 285
Finite-state machines 237
Folding 89
Formal methods 223

Fuzzy control 277
Fuzzy databases 165
Fuzzy extension principle 165
Fuzzy hardware 277
Fuzzy set model 101, 105

GaAs 267
Geographic information systems 177
Global networks 183

Hierarchical locking 161
High-level synthesis 89, 263
Hybrid knowledge 173
Hybrid systems 223
Hypercubes 43

Image processing 285
Indexing structures 177
Information retrieval 101, 105, 173
Inheritance 93
Instruction cache 1
Instruction level parallelism 25
Intelligent knowledge-based systems 129
Interoperability 217

Knowledge representation 191
Knowledge-based system 173

LAN diagnosis 139
Language-prototyping techniques 151
Layout-level design 245
Linear delay systems 201
Linear programming 119
Load balancing 205
Local area networks 205
Logic programming 79, 83

Memory management 79
Metrication 273
Microcontroller 259
Migration tools 129
Module generation 255
Monitoring 281
Multi-domain networks 217
Multi-protocols 209
Multicomputer 59

Multiprocessor systems 115
Multiprocessors 69

Network protocols 111

Object-oriented concurrent programming languages 65
Object-oriented databases 161
Operator 101
Optimization 267
Optimized code 147
Optimizing compiler 25

PCB modern 209
Parallel architecture 83
Parallel compiler generation 147
Parallel debugging 97
Parallel processing 17, 169, 285
Parallel programming 65, 79
Parallel programs 143
Parametrical modules 241
Pattern generation 255
Petri nets 133
Pipeline register file 25
Portability 147
Prefetching 1
Processor architecture 229
Production rules 139
Protocol derivation 213
Protocol specification 191
Protocol synthesis 195
Public Switches Telephone Network (PSTN) 209

Quality standards 273

Real-time systems 119, 223
Realistic faults 245
Relational algebra 169
Relational data model 165
Relational databases 169
Reliability 111
Robotics 17

Scalable 259
Scheduling 89, 119, 223
Security 183
Self-checking structures 237
Service specification 195
Simulation 133, 187, 229
Specifications 93, 97
Spike algorithm 125
Superscalar 75
System architecture 241
System diagnosis 115

Taylor series 201
Technology-independent library 241
Temporal logic 97, 143
Testability enhancement 245
Textual macroprocessor 151
Thesaurus 105
Trace-driven simulation 1
Transbus 59
Transputer systems 115
Transputers 17, 59
Tridiagonal systems 125
True concurrency semantics 143

Unix 205

Vector computers 125
VLIW 25, 75
VLSI 267

Watchdog processors 69

X.500 system 183